PRELIMINARY

Am79468

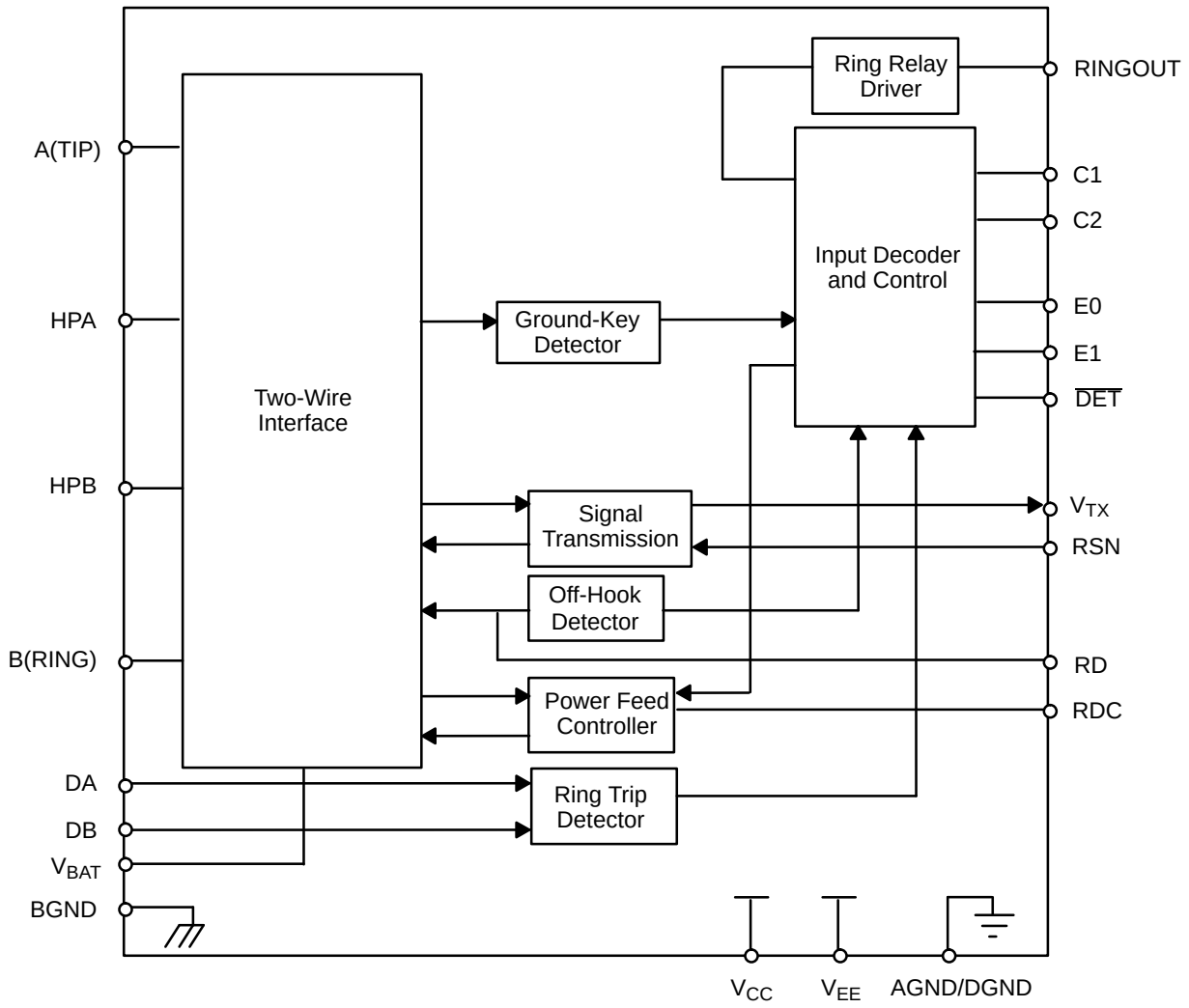
Subscriber Line Interface Circuit

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Programmable constant resistance
- Programmable loop current detector threshold
- Low standby power
- Two-wire impedance set by single external impedance
- On-hook transmission with –50 V to –58 V battery
- On-chip ring relay driver
- Ground-key detector
- Pin and function compatible with Ericsson PBL3762

BLOCK DIAGRAM



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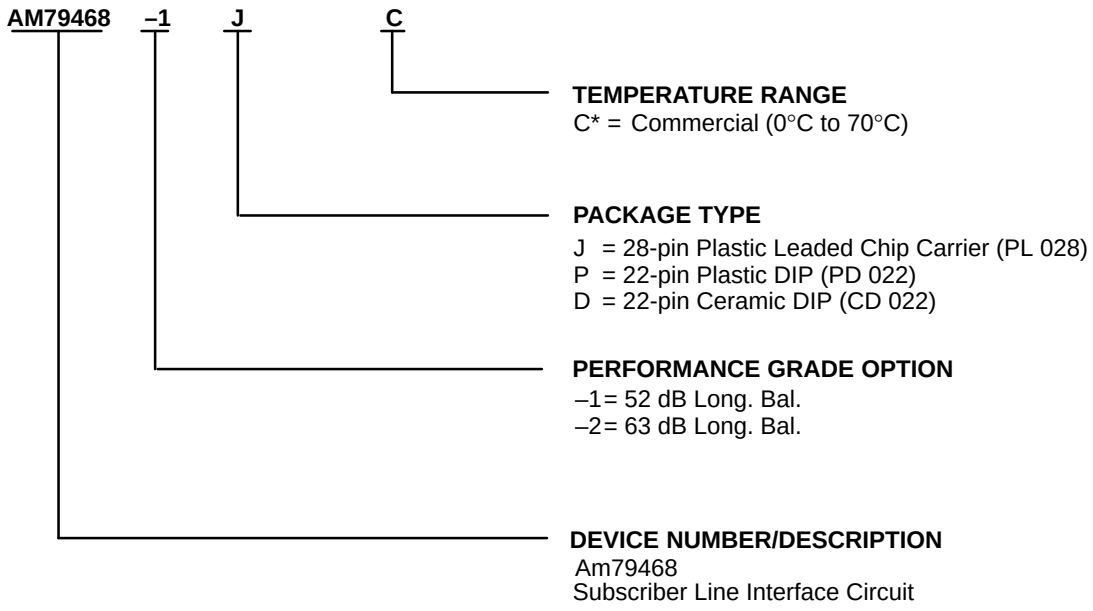
ORDERING INFORMATION

Standard Products

AMD® standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
Am79468	–1	JC
		PC
	–2	DC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

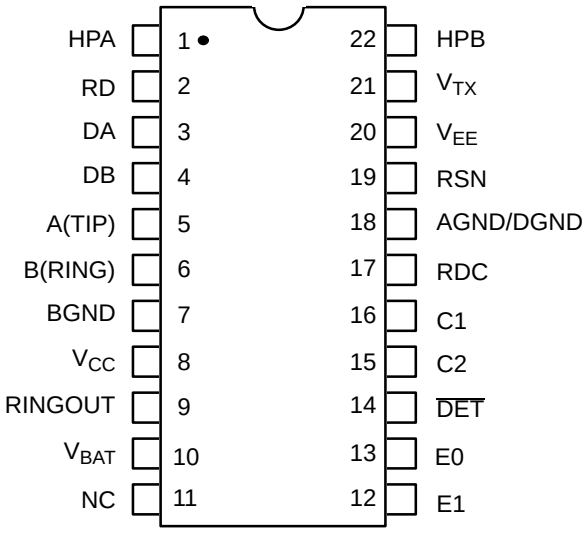
Note:

** Specifications in this data sheet are guaranteed by testing from 0° C to 70° C. Performance from –40° C to +85° C is guaranteed by characterization and periodic sampling of production units.*

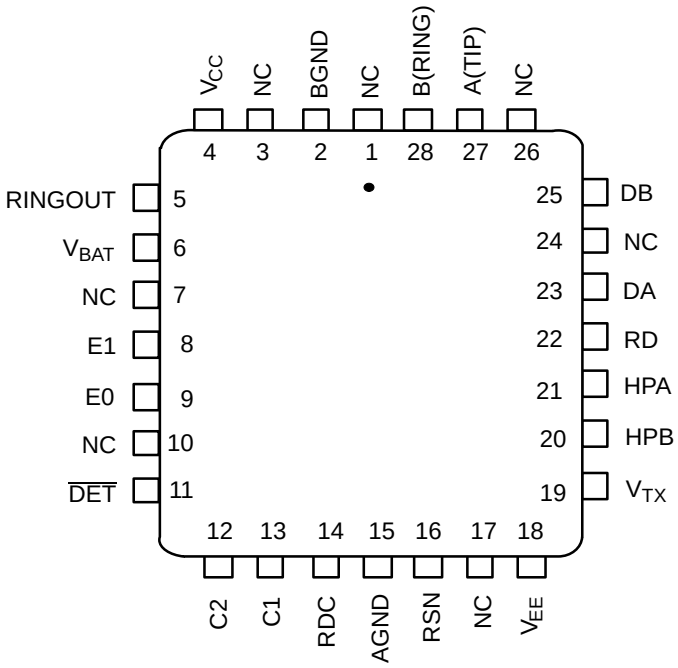
CONNECTION DIAGRAMS

Top View

22-Pin Ceramic DIP



28-Pin PLCC



Notes:

1. *Pin 1 is marked for orientation.*
2. *NC = no connect.*

PIN DESCRIPTION

AGND/DGND
(Ground)

Analog and Digital ground.

A(TIP)
(Output)

Output of A(TIP) power amplifier.

BGND
(Ground)

Battery (power) ground.

B(RING)
(Output)

Output of B(RING) power amplifier.

C2–C1
Decoder (Inputs)

SLIC control pins. C2 is MSB and C1 is LSB. TTL compatible.

DA
Ring Trip Negative (Input)

Negative input to ring trip comparator.

DB
Ring Trip Positive (Input)

Positive input to ring trip comparator.

$\overline{\text{DET}}$
Switch Hook Detector (Output)

When enabled, a logic Low indicates that selected condition is detected. The detect condition is selected by the logic inputs (C1, C2, E0, and E1). The output is open-collector with a built-in 15-kΩ pull-up resistor.

E0
Detector Enable (Input)

A logic High disables $\overline{\text{DET}}$. A logic Low enables $\overline{\text{DET}}$.

E1
Ground Key Enable (Input)

A logic High connects the off-hook/ring trip detector to $\overline{\text{DET}}$, and a logic Low connects the ground key/ring trip detector to $\overline{\text{DET}}$.

HPA

A(TIP) side of high-pass filter capacitor.

HPB

B(RING) side of high-pass filter capacitor.

NC
No Connect

Pin not internally connected.

RD
Detect Resistor Pin

Detector threshold set and filter pin.

RDC
DC Feed Resistor Pin

Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN). The sign of V_{RDC} is minus for normal polarity and plus for reverse polarity.

RINGOUT
Ring relay driver (Output)

Open collector driver with emitter internally connected to BGND.

RSN
Receive Summing Node (Input)

The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 1000 times the current into this pin. The networks that program receive gain, two-wire impedance, and feed resistance all connect to this node.

V_{BAT}

Battery supply.

V_{CC}

+5-V power supply.

V_{EE}

–5-V power supply.

V_{TX}
Transmit Audio (Output)

This output is a unity gain version of the A(TIP) and B(RING) metallic voltage. V_{TX} also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –60°C to +150°C
V_{CC} with respect to AGND/DGND . . . . . 0.5 V to +7 V
V_{EE} with respect to AGND/DGND . . . . . 0.5 V to –7 V
V_{BAT} with respect to AGND/DGND . . . 0.5 V to –70 V
BGND with respect to AGND/DGND . . . . +3 V to –3 V
A(TIP) or B(RING) to BGND:
Continuous . . . . . V_{BAT} to +2 V
10 ms (F = 0.1 Hz) . . . . . V_{BAT} –20 V to +5 V
1 µs (F = 0.1 Hz) . . . . . V_{BAT} –40 V to +10 V
250 ns (F = 0.1 Hz) . . . . . V_{BAT} –70 V to +15 V
Current from A(TIP) or B(RING) . . . . . 70 mA
Current through relay driver . . . . . 50 mA
Ring relay supply voltage . . . . . 0 V to V_{BAT} +75 V
DA and DB inputs
Voltage on ring trip inputs . . . . . V_{BAT} to 0 V
Current into ring trip inputs . . . . . ±5 mA
C1, C2, E0, E1, $\overline{DET}$
Input voltage . . . . . 0 V to V_{CC}
Output voltage ($\overline{DET}$ not active) . . . . . 0 V to V_{CC}
Output current ($\overline{DET}$) . . . . . 5 mA
Power Dissipation (see note) . . . . . T_A = 70°C
Continuous . . . . . 1.5 W
Peak, t <100 ms, t_{REP}> 1 sec . . . . . 4 W

Note: *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See SLIC Packaging Considerations section for more information.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature . . . . . 0°C to +70°C*
V_{CC} . . . . . 4.75 V to 5.25 V
V_{EE} . . . . . –4.75 V to –5.25 V
V_{BAT} . . . . . –50 V to –58 V
AGND/DGND . . . . . 0 V
BGND with respect to
AGND/DGND . . . . . –100 mV to +100 mV

Operating Ranges define those limits between which device functionality is guaranteed.

** Specifications in this data sheet are guaranteed by testing from 0°C to 70°C. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

ELECTRICAL CHARACTERISTICS (See Note 1)

Description	Test Conditions	Preliminary Min	Preliminary Typ	Preliminary Max	Unit	Note
Transmission Performance						
2-wire return loss	200 Hz to 500 Hz 500 Hz to 1 kHz 1.0 kHz to 3.4 kHz	25 27 23			dB dB dB	1,4 1,4 1,4
Z_{VTX}, Analog output impedance	200 Hz to 3.4 kHz		5	20	Ω	
V_{VTX}, Analog output offset voltage	0°C to +70°C –40°C to +85°C	–35 –40		+35 +40	mV mV	 4
Overload level	Load impedance > 20 kΩ	3.1			Vpk	
V_{AB} metallic voltage to V_{TX} voltage gain	300 Hz to 3.4 kHz 0°C to +70°C 300 Hz to 3.4 kHz –40°C to +85°C	0.988 0.980	1.000 1.000	1.012 1.020		 4
Overload level, 2-wire and 4-wire	Z_L = 600 Ω	3.1			Vpk	2
THD, Total Harmonic Distortion	1.0 kHz, 0 dBm		–65	–54	dB	5
THD, on-hook	0 dBm, R_L = 900 Ω, Battery = –51 V			–35.5	dB	5
Longitudinal Performance						
Longitudinal to metallic L-T, L-4 Balance –1 parts	200 Hz to 1 kHz 0°C to +70°C –40°C to +85°C		52 52		dB dB	 4
	1 kHz to 3.4 kHz 0°C to +70°C –40°C to +85°C		52 52		dB dB	 4
Longitudinal to metallic L-T, L-4 Balance –2 parts	200 Hz to 1 kHz 0°C to +70°C –40°C to +85°C		63 55		dB dB	 4
	1 kHz to 3.4 kHz 0°C to +70°C –40°C to +85°C		58 55		dB dB	 4
Longitudinal signal generation 4-L	200 Hz to 4 kHz, normal polarity	45	55		dB	
Longitudinal current capability per wire	Active state	25	35		mArms	
Longitudinal impedance at A or B	0 Hz to 100 Hz		20	35	Ω/wire	
Idle Channel Noise						
C-message weighted noise	2-wire, 0°C to +70°C 2-wire, –40°C to +85°C		+7	+10 +12	dBrnC	 4
	4-wire, 0°C to +70°C 4-wire, –40°C to +85°C		+7	+10 +12	dBrnC	 4
Psophometric weighted noise	2-wire, 0°C to +70°C 2-wire, –40°C to +85°C		–83	–80 –78	dBmp	4 4
	4-wire, 0°C to +70°C 4-wire, –40°C to +85°C		–83	–80 –78	dBmp	4 4
Receive Summing Node (RSN)						
RSN DC voltage	I_{RSN} = 0 mA		0		V	4
RSN impedance	200 Hz to 3.4 kHz		10	20	Ω	4
RSN current to metallic loop current gain	300 Hz to 3.4 kHz 0°C to +70°C –40°C to +85°C	988 980	1000 1000	1012 1020		4 4
Insertion Loss (2-Wire to 4-Wire and 4-Wire to 2-Wire)						
Gain accuracy over temperature	0 dBm, 1 kHz 0°C to +70°C –40°C to +85°C	–0.15 –0.20		+0.15 +0.20	dB dB	3 4
Gain accuracy over frequency	300 Hz to 3400 Hz 0°C to +70°C relative to 1 kHz –40°C to +85°C	–0.10 –0.15		+0.10 +0.15	dB dB	3 4
Gain tracking	+3 dBm to –55 dBm 0°C to +70°C relative to 0 dBm –40°C to +85°C	–0.10 –0.15		+0.10 +0.15	dB dB	3, 4 4

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Preliminary Min	Preliminary Typ	Preliminary Max	Unit	Note
Balance Return Signal (4-Wire to 4-Wire)						
Gain accuracy over temperature	Ref: 0 dBm, 1 kHz 0°C to +70°C –40°C to +85°C	–0.15 –0.20		+0.15 +0.20	dB dB	3 4
Gain accuracy over frequency	300 to 3400 Hz 0°C to +70°C relative to 1 kHz –40°C to +85°C	–0.10 –0.15		+0.10 +0.15	dB dB	3 4
Gain tracking	+3 dBm to –55 dBm 0°C to +70°C relative to 0 dBm –40°C to +85°C	–0.10 –0.15		+0.10 +0.15	dB dB	3, 4 4
Group delay	0 dBm, 1 kHz		5.3		µs	4
Line Characteristics						
Apparent battery voltage	Active mode	47	50	53	V	
I_L, Loop current accuracy	Active mode	$0.925I_L$	I_L	$1.075I_L$	mA	
I_L, Accuracy, standby mode	$I_L = \frac{\lvert V_{BAT} \rvert - 3\ V}{R_L + 1800}$ $T_A = 25°C$	$0.7I_L$	I_L	$1.3I_L$		
I_L, Loop current	Disconnect, $R_L = 0$			100	µA	
I_LLIM ($I_A + I_B$)	Tip and ring shorted to GND		100	130	mA	
V_{AB}, Open circuit voltage	$V_{BAT} = –50$ V	42.8			V	
Power Supply Rejection Ratio (Vripple = 100 mVrms), Active Normal Mode						
V_{CC} V_{EE} V_{BAT}	50 Hz to 3400 Hz 50 Hz to 3400 Hz 50 Hz to 3400 Hz	30 30 35	40 36 41		dB	5 5 5
Effective internal resistance	CAS pin to GND		60		kΩ	4
Loop Detector						
I_T, Loop detect threshold	$R_D = 33$ kΩ, $I_T = 365/R_D$	$0.8I_T$	I_T	$1.2I_T$	mA	
Power Dissipation, Battery = –58 V						
On-hook open circuit			25		mW	
On-hook standby mode			50			
On-hook active mode	$R_L = \infty$, $V_{BAT} = –50$ V		145	300		
Off-hook active mode	$R_L = 0$ Ω $R_L = 300$ Ω $R_L = 600$ Ω		1.5 1.4 1.2	1.8 1.6 1.4	W	
Supply Currents, Battery = –58 V						
I_{CC}, On-hook V_{CC} supply current	Open circuit mode Standby mode Active mode, $V_{BAT} = –50$ V		1.2 1.7 4.8	1.6 2.5 6.5	mA	
I_{EE}, On-hook V_{EE} supply current	Open circuit mode Standby mode Active mode, $V_{BAT} = –50$ V		0.5 0.9 1.9	1.0 1.1 3.0		
I_{BAT}, On-hook V_{BAT} supply current	Open circuit mode Standby mode Active mode, $V_{BAT} = –50$ V		0.3 0.7 2.6	0.9 1.2 4.0		
Ground-Key Detector Thresholds						
I_{TIP} and I_{RING} delta to trigger the ground-key detector		8	12	17	mA	
I_{TIP} and I_{RING} delta to clear the triggered ground-key detector		3	7	12		
Hysteresis		3	5	8		

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Preliminary			Unit	Note
		Min	Typ	Max		
Ring Trip Detector Input						
Bias current		–500	–100		nA	
Offset voltage	Source resistance = 0 to 2 MΩ	–50	0	+50	mV	
Input resistance	Unbalanced Balanced	1 3			MΩ MΩ	4 4
Input common mode range		V_{BAT}		–2	V	
Logic Inputs (C1, C2, E0, E1)						
Input High voltage		2.0		V_{CC}	V	
Input Low voltage		0		0.8		
Input Low current		–500			µA	
Input High current	All inputs except E1	–75		40	µA	
Input High current	Input E1	–75		45	µA	
Logic Output ($\overline{DET}$)						
V_{OH}, Output Low voltage	I_{OUT} = 0.8 mA, 15 kΩ to V_{CC}			0.40	V	
V_{OL}, Output High voltage	I_{OUT} = –0.1 mA, 15 kΩ to V_{CC}	2.4				
Internal pull-up resistor		8		25	kΩ	

Table 1. SLIC Decoding

State	E1	C1	C2	2-Wire Status	Detector Mode	$\overline{DET}$ Output
0	0	0	0	Open circuit	No active detector	Logic level High
1	0	0	1	Active	Ground key detector	Ground key
2	0	1	0	Ringing	No active detector	Logic level High
3	0	1	1	Standby	Ground key detector	Ground key
4	1	0	0	Open circuit	No active detector	Logic level High
5	1	0	1	Active	Loop current detector	Loop current status
6	1	1	0	Ringing	Ring trip detector	Ring trip status
7	1	1	1	Standby	Loop current detector	Loop current status

Note:

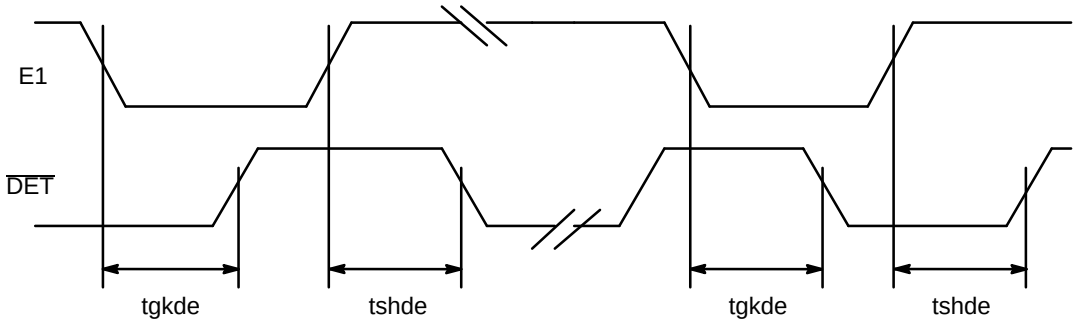
E0 = 1. For E0 = 0, $\overline{DET}$ = logic level High.

SWITCHING CHARACTERISTICS

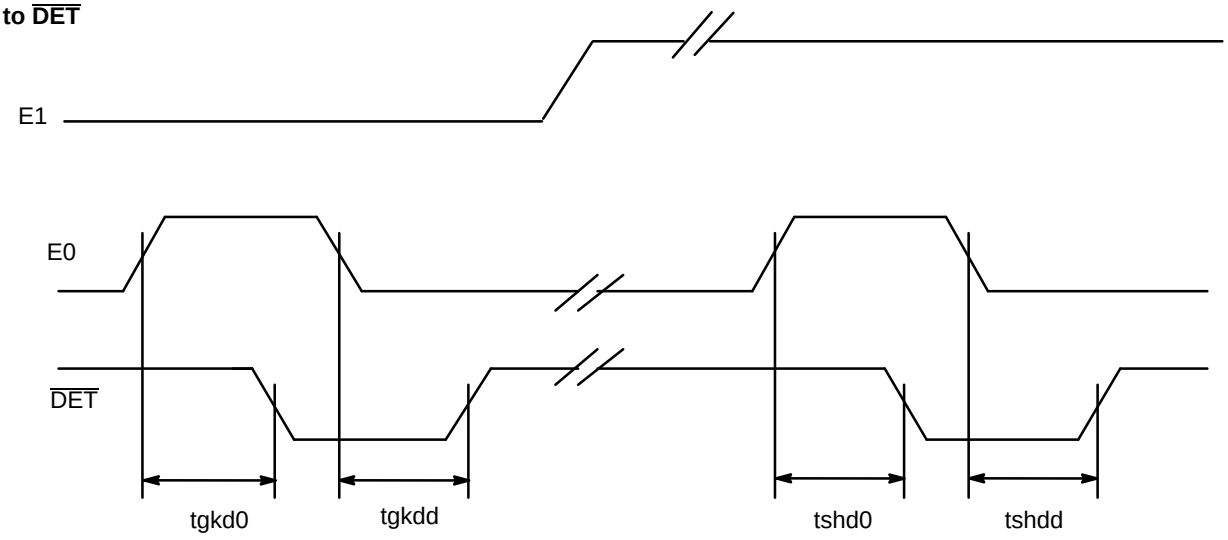
Symbol	Parameter	Test Conditions	Temperature Ranges	Min	Typ	Max	Unit	Note
tgkde	E1 Low to $\overline{DET}$ High (E0 = 1)	Ground key detect mode	0°C to +70°C –40°C to +85°C			3.8 4.0	µs	4 4
	E1 Low to $\overline{DET}$ Low (E0 = 1)	R_L open, R_G connected (See Figure H)	0°C to +70°C –40°C to +85°C			1.1 1.6		4 4
tgkdd	E0 High to $\overline{DET}$ Low (E1 = 0)	Switch hook detect mode R_L = 600 Ω, R_G open (See Figure G)	0°C to +70°C –40°C to +85°C			1.1 1.6	µs	4 4
tgkd0	E0 Low to $\overline{DET}$ High (E1 = 0)		0°C to +70°C –40°C to +85°C			3.8 4.0		4 4
tshde	E1 High to $\overline{DET}$ Low (E0 = 1)	Switch hook detect mode R_L = 600 Ω, R_G open (See Figure G)	0°C to +70°C –40°C to +85°C			1.2 1.7	µs	4 4
	E1 High to $\overline{DET}$ High (E0 = 1)		0°C to +70°C –40°C to +85°C			3.8 4.0		4 4
tshdd	E0 High to $\overline{DET}$ Low (E1 = 1)		0°C to +70°C –40°C to +85°C			1.1 1.6		4 4
tshd0	E0 Low to $\overline{DET}$ High (E1 = 1)		0°C to +70°C –40°C to +85°C			3.8 4.0		4 4

SWITCHING WAVEFORMS

E1 to $\overline{DET}$



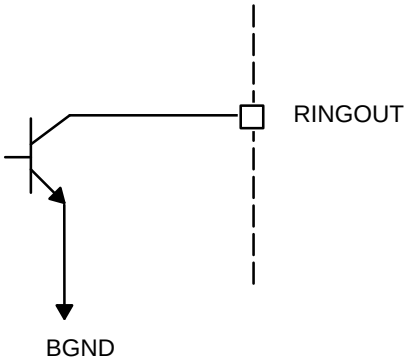
E0 to $\overline{DET}$



Note:

All delays measured at 1.4-V level.

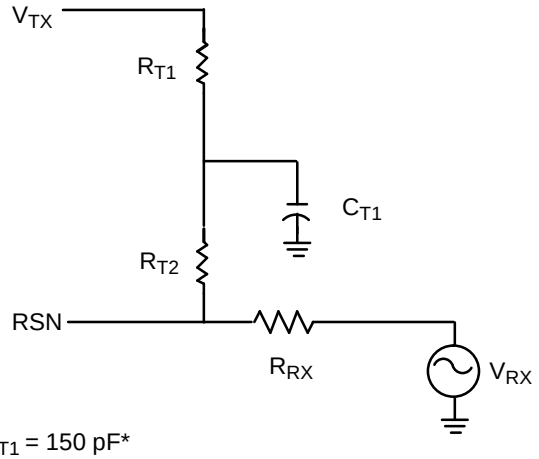
RELAY DRIVER SPECIFICATIONS



Description	Test Conditions	Min	Typ	Max	Unit	Note
Relay Driver Output (RINGOUT)						
On voltage	I_{OL} = 25-mA		+0.2	+0.75	V	
Off leakage	V_{OH} = +12 V			10	µA	

Notes:

1. *Unless otherwise noted, test conditions are:*
   Battery = –52 V, V_{CC} = +5 V, V_{EE} = –5 V, R_L = 600 Ω, C_{HP} = 18 nF, R_{DC1} = R_{DC2} = 20 kΩ, C_{DC} = 0.68 µF, R_D = 33 kΩ, No fuse resistors, two-wire AC input impedance is a 600 Ω resistance synthesized by the programming network shown below.



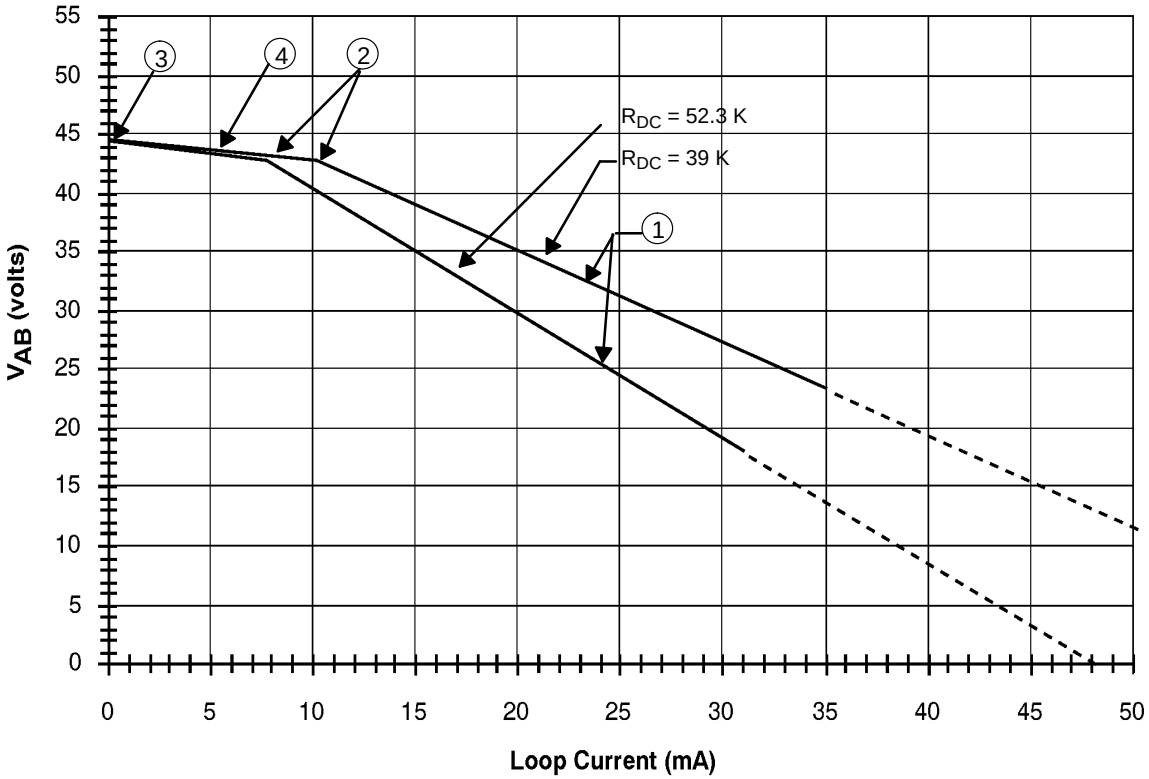
Where: R_{T1} = R_{T2} = R_{RX} = 300 kΩ, C_{T1} = 150 pF*

*C_{T1} is not required when 23 dB two-wire return loss at higher voice frequencies is acceptable. If C_{T1} is not used, R_{T1} and R_{T2} can be combined into one resistor. If this SLIC is used with a DLSAC device, C_{T1} is not required.

2. *Overload level is defined when THD = 1%.*
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes that the two-wire AC load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*

Table 2. User-Programmable Components

$Z_T = 1000\ (Z_{2WIN} - 2R_F)$	Where Z_T is connected between the V_{TX} and RSN pins. The fuse resistors are R_F and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between V_{TX} and RSN must be taken into account.
$Z_{RX} = \frac{Z_T}{2}$	Where Z_{RX} is connected from V_{RX} to the RSN pin and Z_T is defined above. This equation sets the receive gain to 0 dB when the SLIC is terminated with an impedance equal to Z_{2WIN}.
$R_{DC1} + R_{DC2} = 50\ (R_{FEED} - R_{FUSE})$ $C_{DC} = 30\ ms \bullet \frac{1}{R_{DC1}} + \frac{1}{R_{DC2}}$	Where R_{DC1}, R_{DC2} and C_{DC} form the network connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal.
$R_D = \frac{365}{I_T}, \quad C_D = \frac{0.5\ ms}{R_D}$	Where R_D and C_D form the network connected from RD to –5 V and I_T is the threshold current between on-hook and off-hook.



Notes:

1. *Constant resistance feed region:* $V_{AB} = 50 - I_L \frac{R_{DC}}{50}$

2. *Anti-sat cut-in point:* $V_{AB} = 42.7\ V$

3. *Open circuit voltage:* $V_{AB} = 44.5\ V$

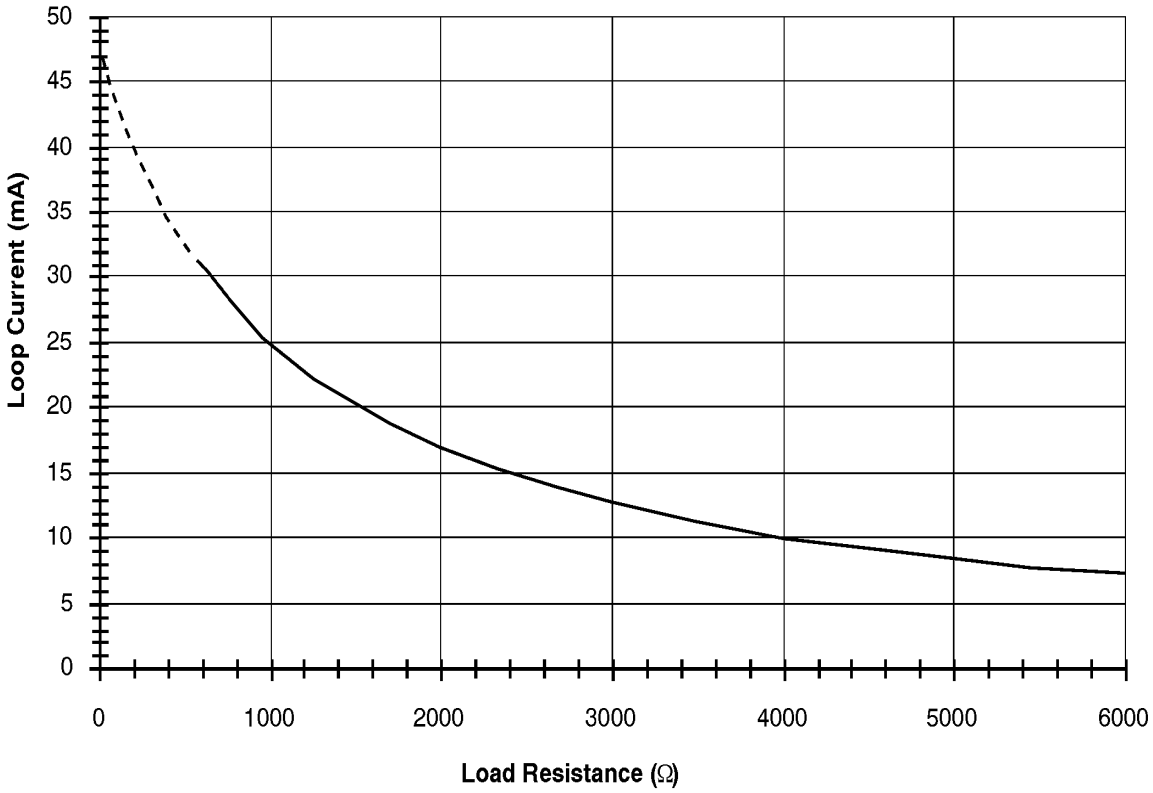
4. *Anti-sat region:* $V_{AB} = 44.5 - I_L \frac{R_{DC}}{200}$

Notes:

a) *There is not any provision for limiting power dissipation on this device. Although it is possible for this SLIC to produce larger currents at low loop resistances, (dotted area of graphs) the design should include a means to prevent the SLIC's power dissipation from exceeding the absolute maximum limits.*

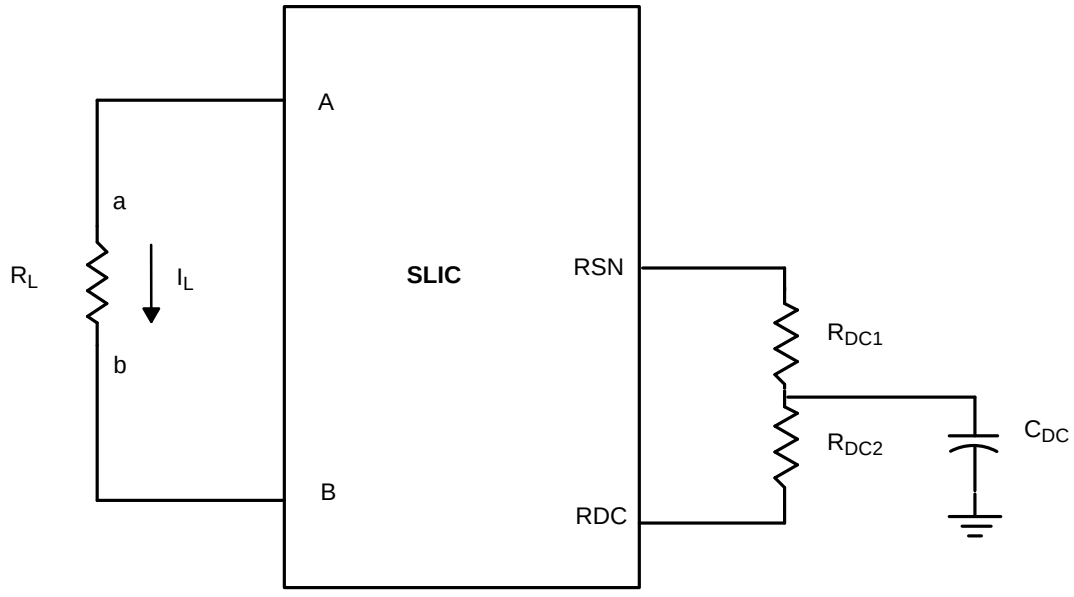
b) *Anti-sat is battery independent. If the V_{BAT} voltage is reduced, it is possible for ac signals to clip as amplifiers begin to saturate. For a given DC feed, the minimum voltage at the V_{BAT} pin must be at least [4.5 V plus peak voltage swing] greater than the DC V_{AB} voltage for that loop condition.*

a. V_A–V_B (V_{AB}) Voltage vs Loop Current (Typical)



R_{DC} = 52.3 K
V_{BAT} > 51.5 V

b. Loop Current vs Load Resistance (Typical)



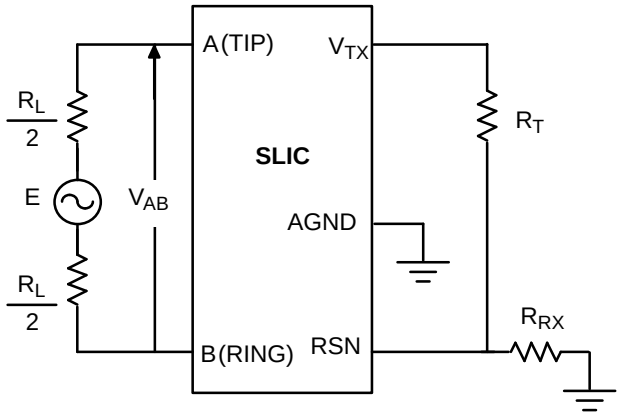
c. Feed Programming

Note:

Feed current programmed by R_{DC1} and R_{DC2}.

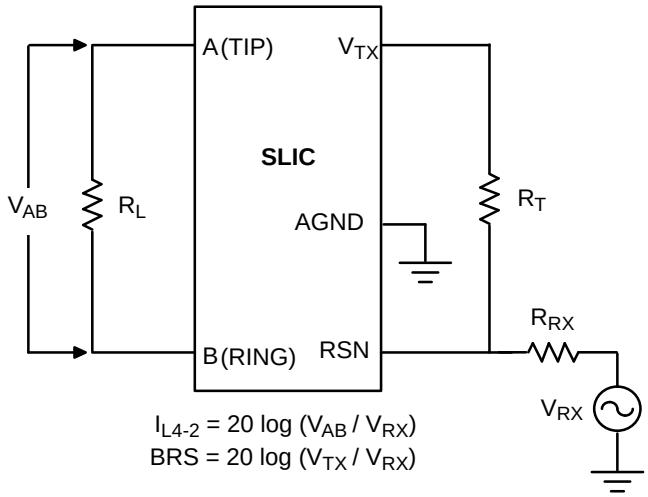
Figure 1. DC Feed Characteristics

TEST CIRCUITS



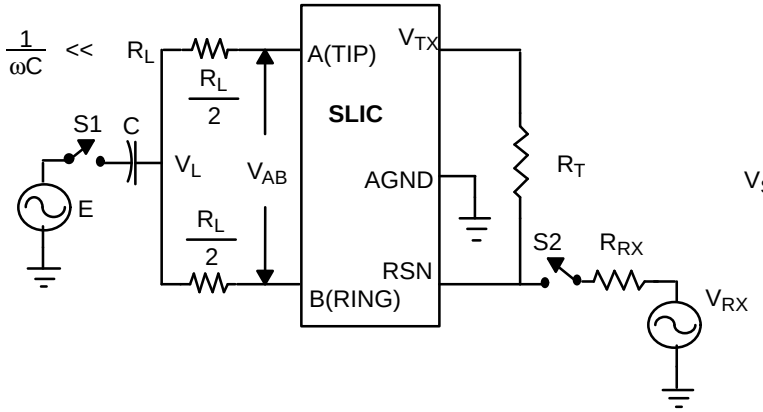
$I_{L2-4} = 20 \log (V_{TX} / V_{AB})$

A. Two-to-Four-Wire Insertion Loss



$I_{L4-2} = 20 \log (V_{AB} / V_{RX})$
$BRS = 20 \log (V_{TX} / V_{RX})$

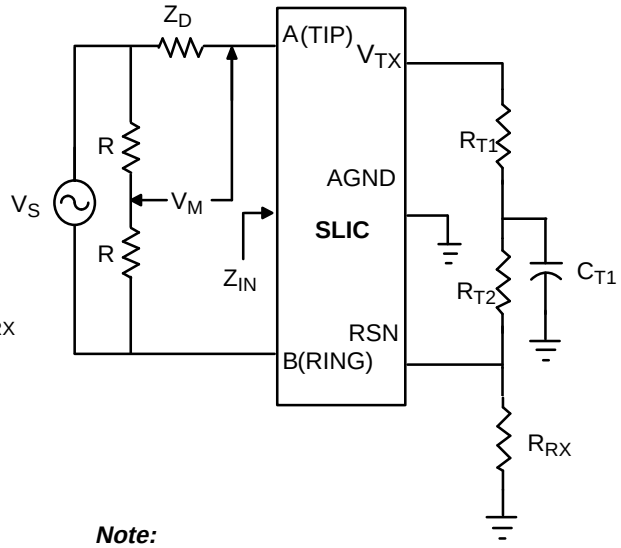
B. Four-to-Two-wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed
L-T Long. Bal. = $20 \log (V_{AB} / E)$
L-T Long. Rej. = $20 \log (V_{TX} / E)$

S2 Closed, S1 Open
4-L Long. Sig. Gen. = $20 \log (V_L / V_{RX})$

C. Longitudinal Balance (IEEE 455-1984)

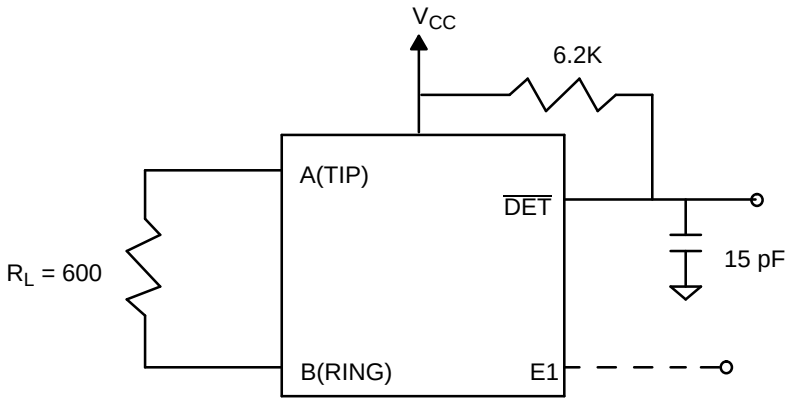


Note:
Z_D is the desired impedance (e.g., the characteristic impedance of the line).

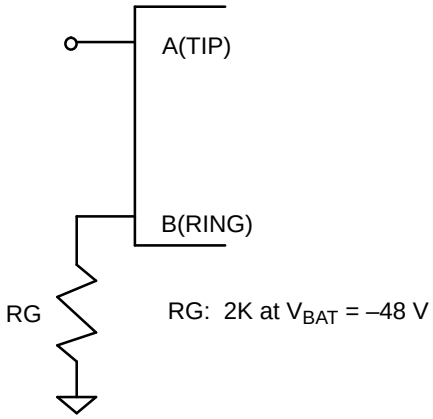
$R_L = -20 \log (2 V_M / V_S)$

D. Two-Wire Return Loss Test Circuit

TEST CIRCUITS (continued)

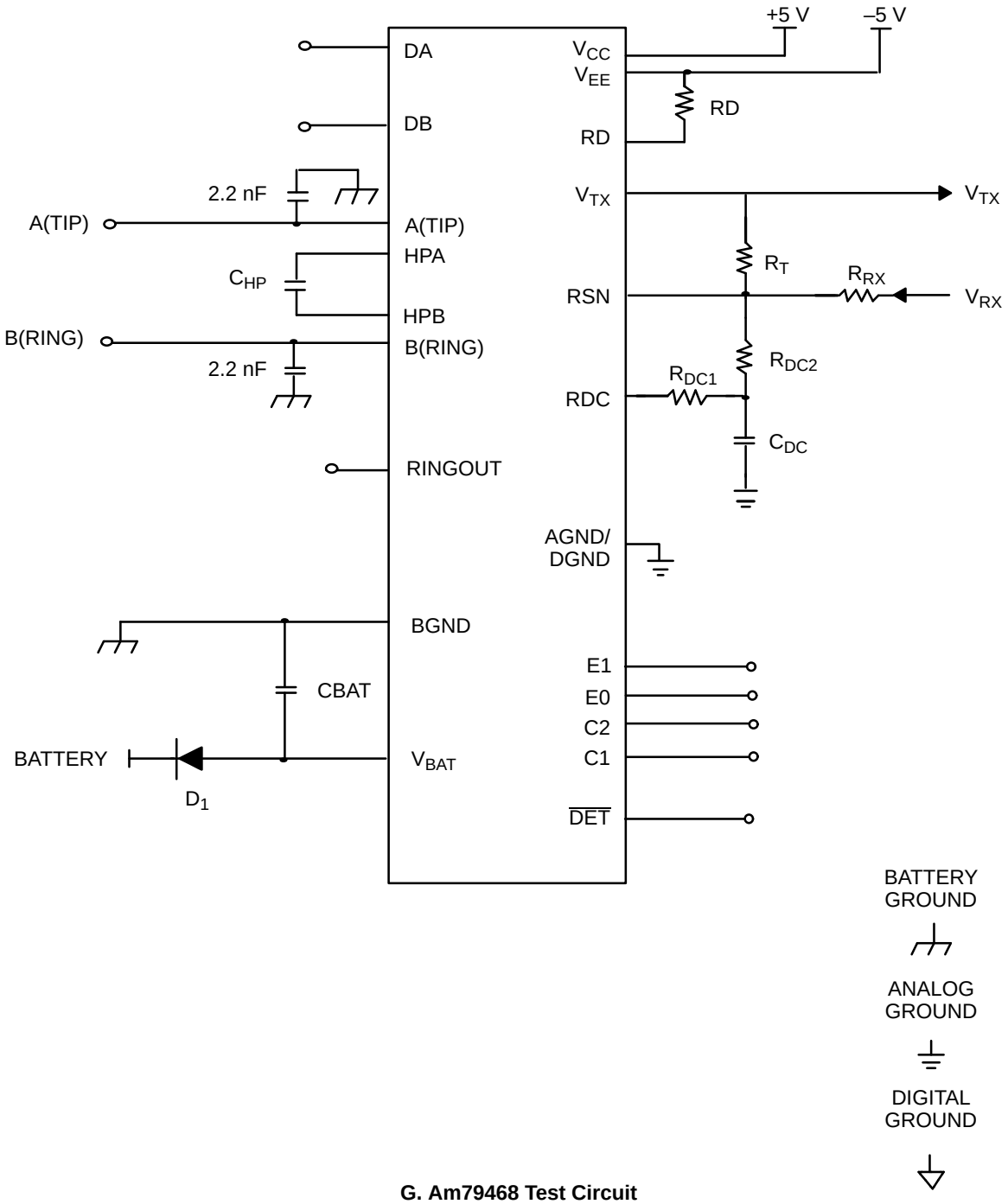


E. Loop Detector Switching



F. Ground-Key Switching

TEST CIRCUITS (continued)



G. Am79468 Test Circuit